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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,982	02/01/2002	Norm Hendrickson	41768/PYI/V165	4215

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EXAMINER	
MEEK, JACOB M	
ART UNIT	**PAPER NUMBER**
2637	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,982	HENDRICKSON, NORM	
	Examiner	Art Unit	
	Jacob Meek	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 -61* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 17, 19, 21 - 24, 29 -31, 33, 42 -46, 48, 55* is/are rejected.

7)☒ Claim(s) *11 -16, 18,20,25 - 28, 34 - 41, 47, 49 - 54, 56 - 61* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/02,6/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1 are objected to because of the following informalities:

Claim 1, 2nd limitation is awkward. Should commas be present between "signal" and "identify", and "transition" and "and".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 – 4, and 21 – 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishida et al (US-5,905,759).

With regard to claim 1, Ishida discloses an RZ recovery system compromising a filter to receive a data signal and to reduce high frequency components from the data signal to form a filtered data signal (see figure 23, 1110 where this is interpreted as equivalent); and recovery unit configured to receive the filtered data signal identify a first type of data transition and provide phase information when 1st type of data transition is identified (see figure 23, 1114 and column 20, lines 39 – 43 where this is interpreted as equivalent).

With regard to claim 2, Ishida discloses a system wherein the 1st type of data transition is a logical 1 to a logical 0 transition (see figure 2, where this is interpreted as equivalent).

With regard to claim 3, discloses teaches a system wherein the 1st type of data transition is a logical 0 to a logical 1 transition (see figure 2, where this is interpreted as equivalent).

With regard to claim 4, Ishida teaches a system wherein the filter is a lowpass filter (see column 6, line 24 – 27).

With regard to claim 4, Ishida teaches a system with a filter (see figure 23, 1110).

With regard to claims 21 – 24, the steps claims as method are a restatement of the function the specific components of the system as claimed above and therefore, it would have been obvious, considering the aforementioned rejection for the system claims 1- 3.

3. Claims 29 - 33, 42, 43, 48, and 55 are rejected under 35 U.S.C. 102(b) as being anticipated by Sun (US-5,056,118).

With regard to claim 29, Sun discloses a method of sampling RZ data compromising determining 1st phase information from a data signal when a 1st type of data transition occurs (see figure 5, RZ, RCLK, F3 and column 11, lines 43 – 54 where this is interpreted as equivalent); determining 2nd phase information from a data signal when a 2nd type of data transition occurs (see figure 5, RZ, RCLK LAG, F1 and column 11, lines 43 – 54 where this is interpreted as equivalent); generating a 1st clock based on 1st phase information (see Figure 3, Recovered Clock and column 10, lines 6- 13); generating a 2nd clock signal based on 2nd phase information (see Figure 3, 56 output column 10, lines 14 - 25 where this is interpreted as equivalent); generating a third clock signal based on the 1st and 2nd clock signals (see Figure 3, 58 output where this is a 3rd clock output based on 1st and 2nd clocks).

With regard to claim 30, Sun teaches the sampling of data based on 3rd clock signal (see figure 3, 50 C input and 58 output).

With regard to claim 31, Sun teaches a method of converting a RZ data signal to and NRZ data signal (see Figure 3).

With regard to claim 32, Sun teaches a method wherein the 3rd clock signal is an interpolation of the 1st and 2nd clock signals (see Figure 3, 58 output where this is a 3rd clock output based on 1st and 2nd clocks and is interpolated with respect to clocks).

With regard to claim 33, Sun discloses RZ data recovery system compromising 1st recovery unit configured to receive a data signal (see figure 4, 54) and identifying a 1st type of data transition and determining 1st phase information when 1st type of data transition is identified (see figure 5,RZ, RCLK and F3 where this is interpreted as equivalent); and 2nd recovery unit configured to receive a data signal (see figure 4, 50) and identifying a 2nd type of data transition and determining 2nd phase information when 2nd type of data transition is identified (see figure 5,RZ, RCLK LAG and F1 where this is interpreted as equivalent).

With regard to claim 42, Sun teaches a 1st type of data transition is a low to high voltage transition (see figure 5, RZ where 1st transition is from low to high).

With regard to claim 43, Sun teaches a 2nd type of data transition is a high to low voltage transition (see figure 5, RZ where 2nd transition is from high to low).

With regard to claim 44, Sun teaches a 1st type of data transition is a rising edge data transition (see figure 5, RZ where 1st transition is from low to high).

With regard to claim 43, Sun teaches a 2nd type of data transition is a falling edge data transition (see figure 5, RZ where 2nd transition is from high to low).

With regard to claim 48, Sun teaches system wherein the 1st recovery unit compromising a 1st phase detector determining phase difference between a 1st recovered clock and the data signal (see figure 4, 54, and figure 5, RZ, RCLK and F3 where this is interpreted as equivalent).

With regard to claim 55, Sun teaches system wherein the 2nd recovery unit compromising a 2nd phase detector determining phase difference between a 2nd recovered clock and the data signal (see figure 4, 50, and figure 5,RZ, RCLK LAG and F1 where this is interpreted as equivalent).

4. Claims 1 – 4, and 21 – 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Gehlot (US-6,404,819).

With regard to claim 1, Gehlot teaches an RZ recovery system compromising a filter to receive a data signal and to reduce high frequency components from the data signal to form a filtered data signal (see figure 2B, D4, D5 and column 6, lines 24 – 27); and recovery unit configured to receive the filtered data signal identify a first type of data transition and provide phase information when 1st type of data transition is identified (see figure 2B, B6 and column 6, lines 27 – 33 where this is interpreted as equivalent)..

With regard to claim 2, Gehlot teaches a system wherein the 1st type of data transition is a logical 1 to a logical 0 transition (see figure 1A, where this is interpreted as equivalent).

With regard to claim 3, Gehlot teaches a system wherein the 1st type of data transition is a logical 0 to a logical 1 transition (see figure 1A, where this is interpreted as equivalent).

With regard to claim 4, Gehlot teaches a system wherein the filter is a lowpass filter (see column 6, line 24 – 27).

With regard to claims 21 – 24, the steps claims as method are a restatement of the function the specific components of the system as claimed above and therefore, it would have been obvious, considering the aforementioned rejection for the system claims 1- 4.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5 – 10, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida ('759).

With regard to claim 5, Ishida teaches a system wherein the data signal is a RZ data signal and the filter is configured to convert the RZ signal into an NRZ signal (see figure 22, 1110 and 1114). Examiner notes that applicant in disclosure has identified the filter operation as including components contained in Ishida's data detection module. In view of the lack of a clear statement of improvement regarding the performance of applicant's invention the particular configuration of components would be a design choice and, therefore, obvious to one of ordinary skill in the art at the time of invention.

With regard to claim 6, Ishida teaches a system wherein the filter qualifies that a logical 1 is valid when a specific voltage level is maintained for a specific amount of time (See figure 22, 1114 and figure 1, 1,3,5 where these elements provide this functionality). Examiner notes that applicant in disclosure has identified the filter operation as including components contained in Ishida's data detection module. In view of lack of a clear statement of improvement regarding the performance of applicant's invention the particular configuration of components would be a design choice and, therefore, obvious to one of ordinary skill in the art at the time of invention.

With regard to claim 7, Ishida teaches a recovery unit adjusting the data signal based on 1st and 2nd data transitions (see figures 9, and 10 and column 2, lines 24 – 27 where this is interpreted as equivalent).

With regard to claim 8, Ishida teaches a phase detector generating a phase difference between a recovered clock signal and the data signal (see Figures 8 – 10 and column 15, lines 46 – 54).

With regard to claim 9, Ishida teaches a system with phase detector generating a phase difference signal based on determined phase difference (see Figure 8 and column 15, lines 46 – 54 where this is interpreted as equivalent functionality).

With regard to claim 10, Ishida teaches a system wherein the phase difference signal is proportional to determined phase difference (see Figure 8 and column 15, lines 46 – 54 where this is interpreted as equivalent functionality).

With regard to claim 17, Ishida teaches a phase detect determining a phase difference between a recovered clock signal and the data signal when a data transition has occurred (see column 11, lines 59 – 66 where this is interpreted as equivalent functionality).

With regard to claim 19, Ishida teaches a recovery unit with an inhibitor receiving the data signal and determines if a data transition has occurred (see column 11, line 66 – column 12, line 7 where this is interpreted as equivalent functionality).

6. Claim 44 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sun ('118).

With regard to claim 44, Sun teaches a low to high voltage transition (see figure 5, RZ where transition is from low to high). Sun is silent with respect to voltage values however, in view of Sun's disclosure the polarity of the circuit would be a design choice and therefore would have been obvious to on of ordinary skill in the art at the time of invention.

Allowable Subject Matter

7. Claims 11 – 16, 18, 20 25 – 28, 34 – 41, 47, 49 – 54, and 56 – 61 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten

in independent form including all of the limitations of the base claim and any intervening claims.

Other Cited Prior Art

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Honacker (US-5,689,530) discloses a device to the recovery of NRZ data from an RZ data stream. Bladh (US-6,324,236) discloses a device for the recovery of NRZ data from a RZ stream including the details of a filtering arrangement. Ibukuro (US 2002/0048069) discloses an optical receiver with many aspects of RZ to NRZ recovery function. Kikuchi (US 6,469,823) discloses an RZ – NRZ converter which teaches aspects of applicant's invention. Tomofuji (US-6,496,552) discloses a phase detection and clocking circuit useful for RZ applications.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Meek whose telephone number is (571)272-3013. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571)272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMM

JAY K. PATEL
SUPERVISORY PATENT EXAMINER